# METHOD AND SYSTEM FOR PROVIDING LOW POWER WLAN RECEIVER

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This invention is related to co-pending application of Jie Liang filed on the same date herewith entitled " Receiver directed power management for WLAN receiver." This application is incorporated herein by reference.

## FIELD OF INVENTION:

[0002] This invention relates to communication systems and in particular to Wireless Local Area Network (WLAN) transceiver system and more particularly to reducing the power usage in WLAN receivers for channel estimation and pilot processing.

## BACKGROUND OF INVENTION:

[0003] Wireless Local Area Networks (WLANs) are becoming very popular today whereby the transceiver may be small and the user no longer needs to be tied to an Ethernet cable. It is also desirable that the communications device such as a wireless transceiver be a mobile battery powered device. The transceiver may be in the form of a lap top computer or a cell phone.

[0004] Because the transceiver is often used without connection to a power source through a power cord, the transceiver is therefore subject to battery drain that limits its use away from a power source. Extending the time period between battery charges is of key importance to continued communications. Various subsystems of a battery powered device may place heavier demands upon battery resources than others.

When the battery powered device employs a wireless transceiver to transmit and receive data, the transceiver typically consumes significant quantities of battery power which impacts battery life.

[0005] In order to increase the overall battery life of such transceivers, power management schemes have been utilized where the communications device enters a sleep mode where only the basic device functions such as system clock, timers, interrupts, etc. are operational. In this mode the device can neither transmit nor receive information and therefore can not perform any communication activities.

[0006] It is desirable to provide a power management system that does not impair the communications capability. Power consumption has become a major performance factor for the WLAN chipset. An important task of the IEEE 802.11a/g standard is the power consumption.

SUMMARY OF INVENTION:

[0007] In accordance with one embodiment of the present invention a method of conserving power in a WLAN receiver includes the operating channel estimation processing for only the preamble portion of each packet and thereafter using the channel estimated value determined during for the duration of the packet.

[0008] In accordance with an embodiment of the present invention the method of conserving power includes the steps of enabling a channel estimator only during the preamble of each packet and running pilot processing after the preamble.

[0009] In accordance with an embodiment of the present invention a system for conserving power in a WLAN receiver includes a channel estimator for detecting

transmitted errors in a transmitted packet and providing equalization for the detected channel errors; a separate pilot processor for detecting off set errors from the channel estimation and providing off set correction to the equalization for the whole data portion of the packet after the preamble and a control response to the start of each packet for enabling the channel estimator during the preamble and thereafter disabling said channel estimator for the remainder of the packet and storing the estimated value.

DESCRIPTION OF DRAWING:

[0010] Figure 1 illustrates a typical WLAN system.

[0011] Figure 2 illustrates OFDM processing duty cycle.

[0012] Figure 3 illustrates a WLAN receiver according to one embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS:

[0013] As illustrated in Figure 1 a typical WLAN network includes a transmitter TX transmitting signals over a wireless channel to a receiver RX. The transmitter TX sends the information in bursts or packets. A typical receiver Rx receives RF signal through a diversity antenna system 21 and processes the RF signal through an RF stage 23 including radio control setting 25, automatic gain control (AGC) 27 and signal diversity selection takes place. The gain control and diversity control are made at the beginning. The receiver usually has two antennas, 21a and 21b, and the one with the strongest signal or signal to noise ratio is selected.

[0014] The output from the RF stage is down converted using a free running local oscillator. The receiver local oscillator is free running and therefore there is usually an

offset frequency from that of the transmitter local oscillator. Here is where a timing estimation and correction is done. The output from the down converter is sampled and converted to digital at an analog to digital concerted (A/D) 29 passes to a Fast Fourier Transform module (FFT) 31 through time domain processing 30. The output from the FFT 31 is applied to the frequency domain processing 33. The output from the FFT is processed for channel compensation due to wireless channel fading, timing errors and frequency offset. The output samples from the FFT 31 are applied to a single clock enabled module 35 enabled for channel estimation and pilot processing. The output from the channel estimation and pilot processing module 35 is applied to time domain processing 30 and frequency domain processing 33. The output from the frequency domain processing 33 is demodulated through demodulation stage 37 and then is decoded at decoder 39, descrambled at descrambler 41 and applied to the MAC interface to the user.

[0015] Each packet starts with a 16 microsecond long preamble followed with data symbols such as symbols 1, 2, 3 etc. Figure 2 illustrates the Orthogonal Frequency Division Multiplexing (OFDM) processing duty cycle. The first eight microseconds (t1-t8) includes the identifier at times t1-t10 during which signal detection, radio control setting, automatic gain control (AGC) and signal diversity selection takes place. During times t8 through t10 coarse frequency estimations are done for timing synchronization. The boundary of the packet is selected. There is a circuit that does a correlation to determine the type of packet as compared to other signals. It determines that it is the start of a standard 802.11 type packet as compared to other signals. At times T1 and T2

channel and fine frequency offset estimation is done. There is a short sequence processing to determine the coarse and fine frequency offset.

[0016] The channel estimation is done on the long sequence portion of the preamble (8 microseconds). The data symbols follow the preamble. The channel is subject to distortions such as from multi-path echo signals. The preamble contains data signals for channel estimation that are sent over the channel to the receiver RX. These data signals are known at the receiver RX. The receiver RX compares the pattern of the received data signals from the channel to the known data signals and determines an estimate of the channel distortions (Hg). The receiver then has an equalizer at the receiver front end that applies an inverted value of the detected channel distortion (1/Hg ) to substantially equalize or remove the distortions based on the channel estimate.

[0017] Also, because the channel may change during the packet a second type of equalization is used is that of pilot processing where in the data symbols to follow the preamble pilot tones are inserted in each symbol for comparing to known tones to measure the error. The system then tracks the channel changes by tracking this pilot to get an offset estimation.

[0018] By analyzing the MIPS (Million Instruction Per Second (MIPS) requirement of the channel estimation and pilot processing algorithms it has been determined that the typical channel estimation algorithm costs more MIPS than pilot tracking. It has been determined that a significant portion of ODFM baseband power is in channel estimation and pilot processing in the single module.

[0019] One implementation of the channel estimation and pilot tracking module is made of a bank of 13 complex Multiply Accumulate (MAC) units. The majority of the

combined channel estimation and pilot processing module power is consumed by these MAC units. Both channel estimation (during long sequence processing- 8 microseconds) and pilot processing during data symbols share the same module.

[0020] The algorithm for channel estimation is y=Ax,

where A is a 52x52 complex matrix, LS (Long Sequence) inverse matrix for a given channel rank

x is 52x1 complex vector, raw channel gain

y is the smooth channel gain for each tone.

[0021] The MIPS estimation where a matrix/vector multiplication is involved:

52x52 complex matrices, 52x1 vector

The computation needs to be completed in about 4 microsecond

The total MIP is 2.5 GOPs (assume 4 real MAC = 1 complex MAC).

[0022] The MIPS requirement for pilot processing according to the algorithm is:

Step 1: Linear regression on each of 4 pilots (phase unwrap)

Step 2: Weighted LS solution for intercept at current symbol (4x2 matrix)

Step 3: Linear regression on the phase offset (intercept) across symbols

Step 4: Calculate Correction factor for each tone (48 tones)

[0023] The MIPS estimation:
Linear Regression: new results can be obtained based on running sum (only add new updates)

Y= b· x + a, then

$$b=\frac{\frac{1}{n}(\sum_{i=1}^{N} x_i \bullet y_i)-\bar{x}\bullet\bar{y}}{\frac{1}{n}\sum_{i=1}^{N} x_i^{\,2}-\bar{x}^{2}}, a=\bar{y}-\bar{b}\bullet\bar{x}$$

MIPS estimation:

Weighted LS solution:

$y = (z^t W z)^{-1} z^t W x$, where

$W \in R4x4$, $z \in R4x2$, $x \in R4x1$,

$y \in R2x1$

Total of 5 linear regression (8 MAC/LR), and 1LS matrix inversion (56 MAC), plus compensation factors (48MAC)

Total MIPS is 36 MIPS.

[0024] The duty cycle of the two processing tasks are very different. The channel estimation needs to be done only once for every packet and the value can be stored in a register and used for the duration of the packet. The pilot processing is active throughout the whole time following the preamble portion. In accordance with the present invention a lot of power saving is achieved if a simpler module can be used exclusively for pilot processing after the preamble and the channel estimator operated only during the preamble of each packet. This control is provided by a state machine identifying when the preamble is finished.

[0025] In accordance with the present invention as illustrated in Figure 3 there is provided the receiver 51 with a separate channel estimator 35a and separate pilot processing 35b and a control logic decode state machine 55 that is response to a new packet to turn on the channel estimator 35a for channel estimation time period only in the preamble and the channel estimation channel estimation module value is stored in a

register and used until the start of a new packet with a preamble. Figure 3 uses the same callouts for the same elements in Figure 1. The elements in Figure 3 that are now controlled are modified to be controllable. The channel estimator 35a receives the data signal sent over the channel and compares this with the known data signals stored in the receiver and determines the channel distortion. The inverse of this channel distortion is then calculated and stored at the output register of the channel estimator 35a to be used to equalize the received signal from the channel. The pilot processing 35b is used throughout the whole data portion after the preamble until the presence of a new packet. The pilot signals are at a set of four frequency bands in the received data signals.

[0026] The block diagram of Figure 3 illustrates that out of the FFT there are two modules 35a and 35b with one for channel estimation only and one for pilot processing only where a power control signal from the decode state machine 55 enables the channel estimate operation only during the preamble of a new packet and the equalization values is stored in the channel estimate register and used through out the packet. The power control signal from the decode state machine 55 enables the pilot processing during the whole data portion of the packet. The pilot processing 35b operates during the whole data period following the preamble and provides new error signal values and correcting values every data symbol. This correcting value from the pilot processing is algebraically summed with that from the channel estimate register. The decode state machine 55 is controlled by the status of the receiver state machine 57. The output from channel estimation and pilot processing is provided to the time domain processing 30 and the frequency domain processing 33 to provide the equalization.

[0027] The pilot processing takes about 1.4% of MIPS compared with channel estimation. A dedicated pilot processing module may use a subset of the MAC units used for channel estimation. One prior art process uses 56 milliwatts. The new process uses only 6 milliwatts with no degradation of performance. The savings is 50 milliwatts.

[0028] Although the invention has been described with reference to specific embodiments, the description is intended to be illustrative of the invention and is not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.